AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1001] on page 1 with the following amended paragraph:

[1001] This application claims benefit [[of]] under 35 U.S.C. § 119(e) of application number 60/467,813, filed May 2, 2003, which is incorporated herein by reference.

Please replace paragraph [1008] on page 2 with the following amended paragraph:

[1008] In one embodiment a method is provided that includes receiving a calibration clock over a terminal; generating at least one correction factor using a control loop to lock an output clock generated by a controllable oscillator to a multiple of the calibration clock; and storing a value corresponding to the at least one correction factor in a ~~non-volatile~~non-volatile memory.

Please replace paragraph [1021] on page 4 with the following amended paragraph:

[1021] Referring to Fig. 1, a high level block diagram of an embodiment of the invention includes an integrated circuit 10, described further herein, coupled to a crystal 11. Both the integrated circuit 10 and the crystal 11 are packaged in a standard ceramic package 15 that is typically utilized for packaging a voltage controlled crystal oscillator (VCXO). Typical packages sizes are 5X7 mm and 9X14 mm. In one embodiment the crystal used is a third overtone 116.64 MHz crystal. Note that another resonating device such as a surface acoustic wave (SAW) device may be utilized in place of crystal 11. The package 15 includes standard input/output signals including a voltage control input 17, a power and ground input, 19 and 21 respectively, clock out plus and minus 23 and an output enable ~~pin and~~ terminal 27.

Please replace paragraph [1024] on page 5 with the following amended paragraph:

[1024] Table 1 shows industry standard input/output (I/O) for four pin and six pin XOs and six pin VCXOs. As can be seen from ~~these~~ Table 1, there is one common static input in all of the packages – the Output Enable/Disable (OE) pin.

Please replace paragraph [1033] on page 7 with the following amended paragraph:

[1033] The device illustrated in Fig. 3 can function as a voltage-controlled crystal/ SAW oscillator (VCXO/VCSO) or as a fixed-frequency clock source (XO/SO). A register bit setting may be used to select between the modes of operation. In voltage-controlled oscillator operational mode the VC analog voltage input port 43 (see Fig. 1) ~~and~~ is coupled to the on-chip analog to digital converter (ADC) 45, which is used to convert VC into the digital frequency control word for the DCO. When operating as a fixed-frequency clock source (XO/SO), the ADC 45 is powered down and its output is fixed to its mid-scale value.

Please replace paragraph [1046] beginning on page 11 with the following amended paragraph:

[1046] The values for dividers 35 (N3), 37 (N2), high speed divider (HS_DIV) 38 (Fig. 4) and 61 (N1) should be selected along with the calibration clock frequency. The equation relating the calibration clock frequency to the output frequency is as follows for one embodiment of the ~~invention.:~~invention:

$f_{OUT} = f_{CALCK} \times N2/(HS\_DIV \times N1)$ (for N3=1), or

$f_{OUT} = f_{CALCK} \times N2/(8 \times HS\_DIV \times N1)$ (for N3=8),

where HS_DIV = [4, 5, 6, 7, 9, 11], $1 \leq N1 \leq 2^7$ and N2 = 256, 512, 1024

Other embodiments may provide other divider values, additional or fewer dividers and thus have different equations for determining the output frequency.

Please replace paragraph [1053] on page 14 with the following amended paragraph:

[1053] Note that calibration can also be performed without a calibration clock input. However, that requires multiple serial data writes to the device to set the correction factor supplied, e.g., through summing node 49 so that while the control voltage [[Vc]]V_c is centered, the clock out signal matches an external calibration clock. By instead using a calibration clock supplied over

the serial port, the device can itself find the desired correction value by locking its PLL to the calibration clock.

Please replace paragraph [1054] beginning on page 15 with the following amended paragraph:

[1054] The on-chip ~~nonvolatile~~non-volatile memory (NVM) 60 provides for permanent storage of device configuration settings and calibration settings at manufacture. The NVM memory space includes bits for all of the settings necessary to fully configure the device. The volatile memory space includes duplicate bits for each NVM bit, plus additional bits that do not require ~~nonvolatile~~non-volatile storage. In one embodiment, the non-volatile memory is one time programmable. A primary (M1) and secondary (M2) NVM space are provided to allow the NVM settings to be written twice during the lifetime of the device. A status register may be used to indicate the current status of M1 and M2. Data is written from volatile memory, such as registers, into NVM using the STORE command. All volatile memory bits with duplicates in the NVM space are written with one command. The first time the STORE command is executed, the M1 NVM space is written. When the write is initiated, a status bit (M1_WR) is permanently set. Once the write is completed, STORE is reset to zero, a read of M1 is done, and the result is compared to the volatile memory settings. If there is a match, then the NVM write has been successful and the M1_CHK status bit is permanently set. The next time the STORE command is executed, the M2 NVM space will be written. After device powerup or reset, the NVM status bits are checked and the appropriate NVM memory space downloaded into the volatile memory. The appropriate NVM space may also be downloaded on command using the RECALL register bit. Once the download is complete, RECALL is reset automatically.

Please replace paragraph [1060] beginning on page 16 with the following amended paragraph:

[1060] In one embodiment the device can store up to six calibration points (frequency and temperature pairs), including the reference point, to calibrate the device across temperature. In normal operation with the temperature compensation feature turned on, the device interpolates between the provided calibration points using a polynomial of order N-1, where N is the ~~umber~~ number of calibration points to be used, which in one embodiment is programmable using register bits. For example, if values are written into RFREQ_11, DELMT1, DELMT2, and DELMT3 while DELMT4 and DELMT5 are not to be used, the user [[set]]sets N=4 so that a 3rd order polynomial interpolation is used.